

YRV32IMAC

RISC-V controller Specification

Yuji Tanaka

E-mail : hge00744@nifty.com

HP : <http://galaxystar.image.coocan.jp/>

1. Introduction

1.1. Specification

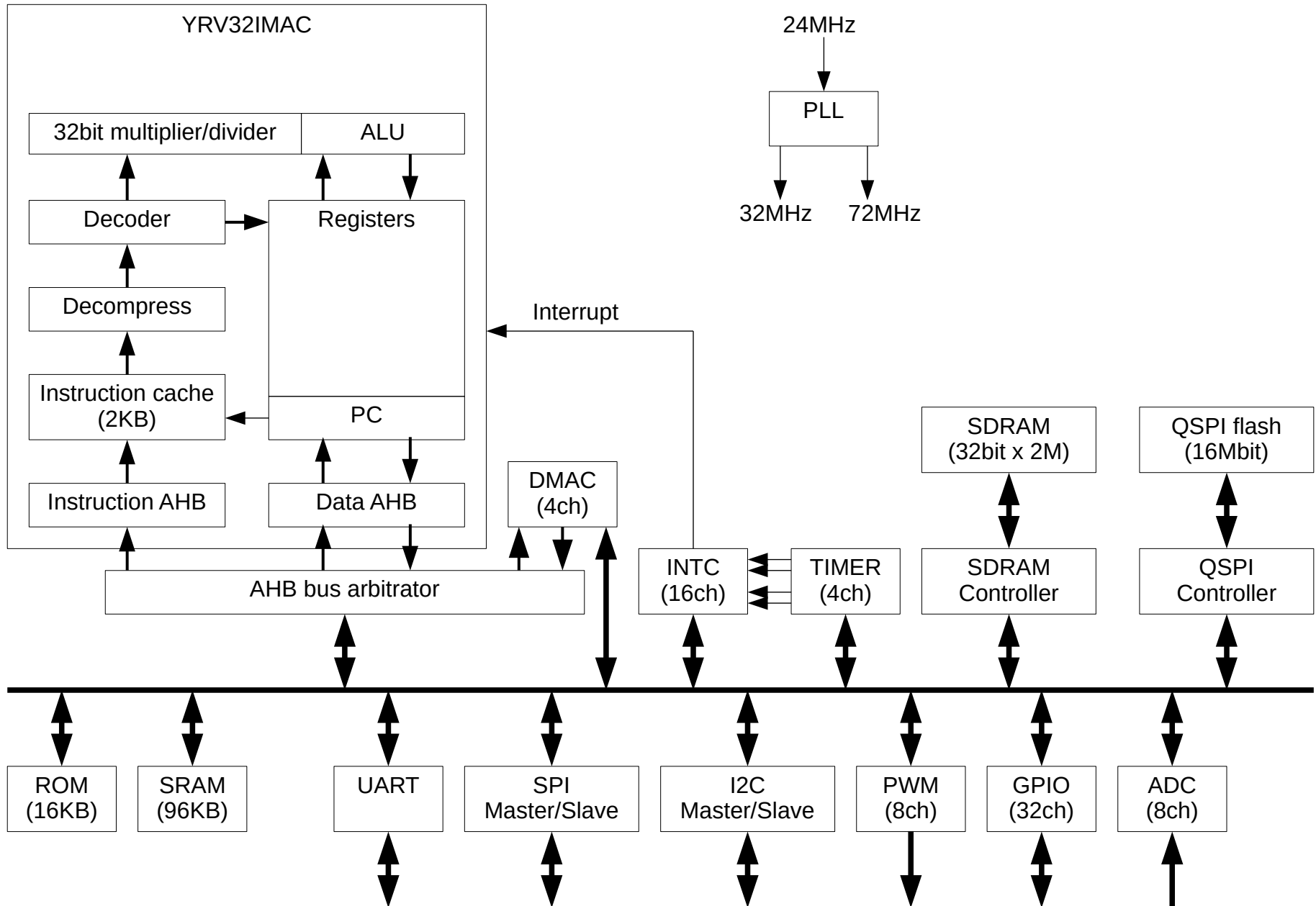
CPU : Original RISC-V core YRV32IMAC
RISC-V RV32IMAC ISA
32MHz
2KB Instruction cache

ROM : 16KB, 0wait
SRAM : 96KB, 0wait
SDRAM : 8MB, 4-5wait
QSPI flash memory : 2MB

DMA : 4ch
INTC : 16ch
UART : 2ch
SPI master/slave : 3ch
I2C master/slave : 2ch
PWM : 8ch
ADC : 8ch
Timer : 4ch
GPIO : 32ch

1. Introduction

1.2. Block Diagram



1. Introduction

1.3. Memory map

Address	Function	Description	Note
01000000h-01017FFFh	RAM(96KB)	0wait	
10010000h	INTC	32ch	
10011000h	TIMER	4ch	Base clock is 32MHz
10012000h	SPI0		Base clock is 32MHz
10012100h	SPI1		Base clock is 32MHz
10012200h	SPI2		Base clock is 32MHz
10012300h	QSPI	QSPI flash memory	Clock is 32MHz
10013000h	UART0		Base clock is 32MHz
10013100h	UART1		Base clock is 32MHz
10014000h	I2C0		Base clock is 32MHz
10014100h	I2C1		Base clock is 32MHz
10015000h	GPIO0	16ch	
10015100h	GPIO1	16ch	
10016000h	PWM0	4ch	Base clock is 32MHz
10016100h	PWM1	4ch	Base clock is 32MHz
10017000h	ADC	8ch, 12bit, About 125ksps	
10018000h	DMAC	SPI-Memory UART-Memory Memory-Memory	
20000000h-20003FFFh	ROM(16KB)	0wait	
60000000h-601FFFFFFh	QSPI flash(2MB)	Single/Dual/Quad support	Clock is 32MHz
80000000h-807FFFFFFh	SDRAM(8MB)	4-5wait	SDRAM clock is 72MHz

1. Introduction

1.4. Implementation

FPGA:ANLOGIC EG4S20BG256

Board:Sipeed Tang Primer

Tool:Tang Dynasty 4.6.25304

Logic size

LUT : 18753 / 19600 (95.68%)

REG : 4473 / 19600 (22.82%)

DSP : 4 / 29 (13.79%)

BRAM 9K : 57 / 64 (89.06%)

BRAM 32K : 16 / 16 (100%)

ADC : 1 / 1 (100%)

Timing

clk_32M : 35.117ns, 28.476MHz (Real frequency : 32MHz)

clk_dram : 8.337ns, 119.947MHz (Real frequency : 72MHz)

2. Pin assign

2.1. Pin list

Terminal	Function1	Function2	Note
K14(CLKIN)	Clock(i)		24MHz
K16(USER_KEY)	Reset(i)		Reset
D3(QSPI_CS)	QSPI_CS(o)		QSPI flash memory
B3(QSPI_DQ[0])	QSPI_DQ[0](io)		QSPI flash memory
F4(QSPI_DQ[1])	QSPI_DQ[1](io)		QSPI flash memory
F5(QSPI_DQ[2])	QSPI_DQ[2](io)		QSPI flash memory
B1(QSPI_DQ[3])	QSPI_DQ[3](io)		QSPI flash memory
H4(QSPI_SCK)	QSPI_CLK(o)		QSPI flash memory
H13	UART0_RXD(i)		UART
J13	UART0_TXD(o)		UART
J11	GPIO0[2](io)	PWM0[0](o)	
L12	GPIO0[3](io)	PWM0[1](o)	
F16	GPIO0[4](io)	PWM0[2](o)	
E16	GPIO0[5](io)	PWM0[3](o)	
C15	GPIO0[6](io)	PWM1[0](o)	
C16	GPIO0[7](io)	PWM1[1](o)	
B16	GPIO0[8](io)	PWM1[2](o)	
B15	GPIO0[9](io)	PWM1[3](o)	
A14	GPIO0[10](io)	SPI0_M_XS(o) / SPI0_S_XS(i)	
B14	GPIO0[11](io)	SPI0_M_MOSI(o) / SPI0_S_MOSI(i)	
B10	GPIO0[12](io)	SPI0_S_MISO(o) / SPI0_M_MISO(i)	
A3	GPIO0[13](io)	SPI0_M_C(o) / SPI0_S_C(i)	
T13	GPIO0[14](io)		
P8	GPIO0[15](io)		

2. Pin assign

Terminal	Function1	Function2	Note
P9	GPIO1[0](io)		
R9	GPIO1[1](io)		
T15	GPIO1[2](io)	I2C0_SDA(io)	
R12	GPIO1[3](io)	I2C0_SCL(io)	
T14	GPIO1[4](io)	I2C1_SDA(io)	
R14	GPIO1[5](io)	I2C1_SCL(io)	
R7	GPIO1[6](io)	UART1_RXD(i)	
T7	GPIO1[7](io)	UART1_TXD(o)	
P5	GPIO1[8](io)	SPI1_M_XS(o) / SPI1_S_XS(i)	
N5	GPIO1[9](io)	SPI1_M_MOSI(o) / SPI1_S_MOSI(i)	
R2	GPIO1[10](io)	SPI1_S_MISO(o) / SPI1_M_MISO(i)	
P2	GPIO1[11](io)	SPI1_M_C(o) / SPI1_S_C(i)	
N3	GPIO1[12](io)		
M4	GPIO1[13](io)		
D5	GPIO1[14](io)		
D6	GPIO1[15](io)		
J14(LED_B)	GPIO1[13](o)		RGB LED
R3(LED_R)	GPIO1[14](o)		RGB LED
P13(LED_G)	GPIO1[15](o)		RGB LED

3. CPU

3.1. Specification

ISA : RISC-V RV32IMAC

Pipeline : 4 stage (Fetch, Decompress, Decode, Execute)

Cache : 2KB Instruction cache

Instruction bus : 32bit AHB

Data bus : 32bit AHB

Multiplier/Divider :

32bit x 32bit → 64bit 3clk

32bit / 32bit → 32bit ... 32bit 2-17clk

Clock : 32MHz

4. Memory

4.1. Specification

ROM : 32bit x 4K, Read only, 0wait

SRAM : 32bit x 24K, Read/Write, 0wait

SDRAM : 32bit x 2M, Read/Write, 3-4wait

QSPI flash memory : 32bit x 512K, Read (Programable), 25-65wait

All memory support 8bit/16bit/32bit access.

5. DMAC (Direct Memory Access Controller)

5.1. Specification

Memory mapped data to memory mapped data transfer only.
(Address increment / decrement / fix)

Support peripheral : SPI, UART

Support 8bit/16bit/32bit data width.

Maximum transfer data size is 65536.

Channel : 4ch

5. DMAC (Direct Memory Access Controller)

5.2. Register map

Address	Register	Function	Initial value	Note
10018000h	MODE0[15:0]	[0]:Enable 0-disable 1-enable [1]:Direction 0-IO->Memory 1-Memory->IO [3:2]:Read data width 00-8bit 01-16bit 10-32bit [6:5]:Write data width 00-8bit 01-16bit 10-32bit [9:8]:Read address 00/11-fix 01-inc 10-dec [11:10]:Write address 00/11-fix 01-inc 10-dec [15:12]:Request select	0000h	Please set same value to [3:2] and [6:5].
10018004h	READ_ADD0[31:0]	Ch0 Read address	00000000h	
10018008h	WRITE_ADD0[31:0]	Ch0 Write address	00000000h	
1001800Ch	NUMBER0[15:0]	Ch0 transfer data number	0000h	
10018010h	MODE1[15:0]	Ch1 mode (Same as MODE0)	0000h	
10018014h	READ_ADD1[31:0]	Ch1 Read address	00000000h	
10018018h	WRITE_ADD1[31:0]	Ch1 Write address	00000000h	
1001801Ch	NUMBER1[15:0]	Ch1 transfer data number	0000h	
10018020h	MODE2[15:0]	Ch2 mode (Same as MODE0)	0000h	
10018024h	READ_ADD2[31:0]	Ch2 Read address	00000000h	
10018028h	WRITE_ADD2[31:0]	Ch2 Write address	00000000h	
1001802Ch	NUMBER2[15:0]	Ch2 transfer data number	0000h	
10018030h	MODE3[15:0]	Ch3 mode (Same as MODE0)	0000h	
10018034h	READ_ADD3[31:0]	Ch3 Read address	00000000h	
10018038h	WRITE_ADD3[31:0]	Ch3 Write address	00000000h	
1001803Ch	NUMBER3[15:0]	Ch3 transfer data number	0000h	

5. DMAC (Direct Memory Access Controller)

5.3. DMAC request

Number	Request	Direction	Function	Note
0	SPI0_TX	Mem->IO	SPI TX (WRITE_ADD=10012018h, 10012038h)	
1	SPI0_RX	IO->Mem	SPI RX (READ_ADD=10012018h, 10012038h)	
2	SPI1_TX	Mem->IO	SPI TX (WRITE_ADD=10012118h, 10012138h)	
3	SPI1_RX	IO->Mem	SPI RX (READ_ADD=10012118h, 10012138h)	
4	SPI2_TX	Mem->IO	SPI TX (WRITE_ADD=10012218h, 10012238h)	
5	SPI2_RX	IO->Mem	SPI RX (READ_ADD=10012218h, 10012238h)	
6	-	-		
7	-	-		
8	UART0_TX	Mem->IO	UART TX (WRITE_ADD=1001300Ch)	
9	UART0_RX	IO->Mem	UART RX (READ_ADD=1001300Ch)	
10	UART1_TX	Mem->IO	UART TX (WRITE_ADD=1001310Ch)	
11	UART1_RX	IO->Mem	UART RX (READ_ADD=1001310Ch)	
12	Always 1	Mem->Mem	To transfer from memory to memory.	
13	Always 1	Mem->Mem	To transfer from memory to memory.	
14	Always 1	Mem->Mem	To transfer from memory to memory.	
15	Always 1	Mem->Mem	To transfer from memory to memory.	

6. INTC (Interrupt Controller)

6.1. Specification

Level / edge and rise / fall select.

Channel : 16ch

6.2. Register map

Address	Register	Function	Initial value	Note
10010000h	REQUEST[15:0](R) CLEAR[15:0] (W)	[15:0](R):Interrupt request 0-No request 1-Request [15:0](W):Interrupt clear for edge mode 0-Not clear 1-Clear	0000h	
10010004h	MASK[15:0]	[15:0]:Interrupt mask 0-disable 1-enable	0000h	
10010008h	MODE[15:0]	[15:0]:Mode 0-level 1-edge Level mode : Clear request of the controller. Edge mode : Clear request by CLEAR register.	0000h	
1001000Ch	EDGE[15:0]	[15:0]:Edge 0-fall 1-rise	0000h	

6. INTC (Interrupt Controller)

6.3. INTC request

Bit number	Request	Edge/Level	Function	Note
0	-			
1	-			
2	-			
3	-			
4	TIMER0	Edge	Timer	
5	TIMER1	Edge	Timer	
6	TIMER2	Edge	Timer	
7	TIMER3	Edge	Timer	
8	-			
9	-			
10	-			
11	-			
12	-			
13	-			
14	-			
15	-			

7. TIMER (Timer controller)

7.1. Specification

8bit pre-scaler and 16bit timer.

Repeat and one shot.

All timers connect to INTC.

Channel : 4ch

7.2. Register map

Address	Register	Function	Initial value	Note
10011000h	PRE_SCALER[7:0]	[7:0]:Pre-scaler Timer clock=Clock frequency / (PRE_SCALER+1)	00h	Clock frequency is 32MHz.
10011004h	ENABLE[3:0]	[3:0]:Enable 0-disable 1-enable	0h	
10011008h	MODE[3:0]	[3:0]:Mode 0-Repeat 1-one shot	0h	
1001100Ch	READ_SEL[3:0]	[3:0]:COUNT? read data select 0-Timer count 1-Write value	0h	
10011010h	COUNT0[15:0]	[15:0]:Ch0 count value	0000h	READ_SEL[0]
10011014h	COUNT1[15:0]	[15:0]:Ch1 count value	0000h	READ_SEL[1]
10011018h	COUNT2[15:0]	[15:0]:Ch2 count value	0000h	READ_SEL[2]
1001101Ch	COUNT3[15:0]	[15:0]:Ch3 count value	0000h	READ_SEL[3]

8. SPI (Serial Peripheral Interface)

8.1. Specification

8bit pre-scaler (Min. 2)

Support 1-32bit command and 1-16bit data

16 words FIFO.

Master / slave

Channel : 1ch

8. SPI (Serial Peripheral Interface)

8.2. Register map

Address	Register	Function	Initial value	Note
10012000h 10012100h 10012200h	RATE[7:0]	[7:0]:RATE (0 means 1.) Frequency=Clock frequency / (RATE+1)	00h	Clock frequency is 32MHz.
10012004h 10012104h 10012204h	COMMAND_LEN[5:0]	[5:0]:Command length (1-32)	00h	
10012008h 10012108h 10012208h	M_COMMAND[15:0]	[31:0]:Command(Transfer)	0000h	
1001200Ch 1001210Ch 1001220Ch	M_COMMAND[31:16]		0000h	
10012010h 10012110h 10012210h	DATA_LEN[4:0]	[4:0]:Data length (1-16)	00h	
10012014h 10012114h 10012214h	M_MODE[5:0]	[0]:Enable 0-disable 1-enable [1]:Buffer full 0-Not full 1-Full [2]:Busy 0-Buffer empty and transter end 1-Busy [5]:Receive data valid 0-No data 1-valid	0000h	
10012018h 10012118h 10012218h	M_DATA[15:0]	[15:0](R):RX data [15:0](W):TX data	0000h	

8. SPI (Serial Peripheral Interface)

Address	Register	Function	Initial value	Note
10012024h 10012124h 10012224h	S_COMMAND[15:0]	[31:0]:Command(Receive)	0000h	
1001202Ch 1001212Ch 1001222Ch	S_COMMAND[31:16]		0000h	
10012034h 10012134h 10012234h	S_MODE[5:0]	[0]:Enable 0-disable 1-enable [1]:Buffer full 0-Not full 1-Full [2]:Busy 0-Buffer empty and transter end 1-Busy [5]:Receive data valid 0-No data 1-valid	00h	
10012038h 10012138h 10012238h	S_DATA[15:0]	[15:0](R):RX data [15:0](W):TX data	0000h	

9. QSPI (Quad Serial Peripheral Interface)

9.1. Specification

QSPI flash memory is mapped as 32bit memory.

Support single / dual / quad and address width 8 / 16 / 24 / 32bit.

Support SPI master.

No rate counter. (Clock frequency is fixed.)

Channel : 1ch

9. QSPI (Quad Serial Peripheral Interface)

9.2. Register map

Address	Register	Function	Initial value	Note
10012300h	DATA[31:0]	[31:0](R):RX command / data [31:0](W):TX command / data	00000000h	
10012304h	DATA_LEN[5:0]	[5:0]:Command / data length (1-32)	00h	
10012308h	MODE[1:0]	[1:0]:Mode 00-Single 01-Dual 1x-Quad	0h	
1001230Ch	ENABLE[7:0]	[0]:Enable 0-Enable and /CS=0 1-Disable [1]:Send 0-Not send 1-Send [2]:Receive 0-Not receive 1-Receive [4]:/WP output value [5]:/WP output enable 0-Hi-Z 1-Output [6]:/HOLD output value [7]:/HOLD output enable 0-Hi-Z 1-Output	00h	
10012310h	ROM_READ[7:0]	[7:0]:ROM read command	BBh	Read dual
10012314h	ROM_WRITE[7:0]	[7:0]:ROM write command	02h	
10012318h	ROM_MODE0[7:0]	[1:0]:ROM read address 00-Single 01-Dual 1x-Quad [3:2]:ROM read data 00-Single 01-Dual 1x-Quad [5:4]:ROM write address 00-Single 01-Dual 1x-Quad [7:6]:ROM write data 00-Single 01-Dual 1x-Quad	05h	
1001231Ch	ROM_MODE1[5:0]	[1:0]:ROM read dummy clock 00-0bit 01-8bit 10-16bit 11-24bit [5:4]:ROM address width 00-8bit 01-16bit 10-24bit 11-32bit	21h	

10. UART (Universal Asynchronous Receiver Transceiver)

10.1. Specification

16Bit rate counter.

Data width 4-8bit, party non / even / odd, stop 1bit / 2bit

16 words FIFO

Channel : 1ch

10.2. Register map

Address	Register	Function	Initial value	Note
10013000h 10013100h	RATE[15:0]	[15:0]:Baudrate (0 means 1) baudrate=Clock frequency / (RATE+1)	0000h	Clock frequency is 32MHz.
10013004h 10013104h	MODE[5:0]	[2:0]:Data width 000-8bit 001-7bit 010-6bit 011-5bit 1xx-4bit [3]:Stop bit 0-1bit 1-2bit [5:4]:Parity 0x-non 10-even 11-odd	00h	
10013008h 10013108h	STATUS[4:0]	[0]:Buffer full 0-Not full 1-Full [1]:TX busy 0-Not busy 1-Busy [4]:RX valid data 0-No data 1-valid	00h	
1001300Ch 1001310Ch	DATA[7:0]	[7:0](R):RX data [7:0](W):TX data	00h	

11. I2C (Inter-Integrated Circuit controller)

11.1. Specification

8bit rate counter.

Master / Slave

Channel : 1ch

11. I2C (Inter-Integrated Circuit controller)

11.2. Register map

Address	Register	Function	Initial value	Note
10014000h 10014100h	RATE[7:0]	[7:0]:Rate (0 means 1) Frequency=Clock frequency / (RATE+1)	0000h	Clock frequency is 32MHz.
10014004h 10014104h	DEVICE_ADD[7:0]	[7:1]:Device address	00h	
10014008h 10014108h	M_ENABLE[7:0]	Master mode [0]:Enable 0-Disable 1-Enable [1]:TX buffer full 0-Not full 1-Full [2]:Busy 0-Not busy 1-Busy [5]:RX valid data 0-No data 1-valid [6]:Data no ack 0-ack 1-nak [7]:Address no ack 0-ack 1-nak	00h	
1001400Ch 1001400Ch	M_DATA[7:0]	Master mode [7:0](R):RX data [7:0](W):TX data	00h	
10014018h 10014118h	S_ENABLE[5:0]	Slave mode [0]:Enable 0-Disable 1-Enable [1]:TX buffer full 0-Not full 1-Full [2]:Busy 0-Not busy 1-Busy [5]:RX valid data 0-No data 1-valid	00h	
1001401Ch 1001411Ch	S_DATA[7:0]	Slave mode [7:0](R):RX data [7:0](W):TX data	00h	

12. GPIO (General Purpose Input / Output)

12.1. Specification

Select input / output.

Select port functions.

Channel : 16ch

12.2. Register map

Address	Register	Function	Initial value	Note
10015000h 10015100h	OUTPUT[15:0]	[15:0]:Output value	0000h	Valid at DIRECTION[n]=0
10015004h 10015104h	INPUT[15:0](R)	[15:0](R):Input value	xxxx	
10015008h 10015108h	DIRECTION[15:0]	[15:0]:Select input / output. 0-Output 1-Input	FFFFh	
1001500Ch 1001510Ch	FUNCTION[15:0]	[15:0]:Function 0-GPIO 1-Other function	0000h	

12. GPIO (General Purpose Input / Output)

12.3. GPIO0 function

Bit number	Terminal	FUNCTION[n]=0	FUNCTION[n]=1	Note
0	H13	UART0_RXD(i)	UART0_RXD	
1	J13	UART0_TXD(o)	UART0_TXD	
2	J11	GPIO0[2](io)	PWM0[0]	
3	L12	GPIO0[3](io)	PWM0[1]	
4	F16	GPIO0[4](io)	PWM0[2]	
5	E16	GPIO0[5](io)	PWM0[3]	
6	C15	GPIO0[6](io)	PWM1[0]	
7	C16	GPIO0[7](io)	PWM1[1]	
8	B16	GPIO0[8](io)	PWM1[2]	
9	B15	GPIO0[9](io)	PWM1[3]	
10	A14	GPIO0[10](io)	SPI0_M_XS(o) / SPI0_S_XS(i)	
11	B14	GPIO0[11](io)	SPI0_M_MOSI(o) / SPI0_S_MOSI(i)	
12	B10	GPIO0[12](io)	SPI0_S_MISO(o) / SPI0_M_MISO(i)	
13	A3	GPIO0[13](io)	SPI0_M_C(o) / SPI0_S_C(i)	
14	T13	GPIO0[14](io)	GPIO0[14](io)	
15	P8	GPIO0[15](io)	GPIO0[15](io)	

12. GPIO (General Purpose Input / Output)

12.4. GPIO1 function

Bit number	Terminal	FUNCTION[n]=0	FUNCTION[n]=1	Note
0	P9	GPIO1[0](io)	GPIO1[0](io)	
1	R9	GPIO1[1](io)	GPIO1[1](io)	
2	T15	GPIO1[2](io)	I2C0_SDA(io)	
3	R12	GPIO1[3](io)	I2C0_SCL(io)	
4	T14	GPIO1[4](io)	I2C1_SDA(io)	
5	R14	GPIO1[5](io)	I2C1_SCL(io)	
6	R7	GPIO1[6](io)	UART1_RXD(i)	
7	T7	GPIO1[7](io)	UART1_TXD(o)	
8	P5	GPIO1[8](io)	SPI1_M_XS(o) / SPI1_S_XS(i)	
9	N5	GPIO1[9](io)	SPI1_M_MOSI(o) / SPI1_S_MOSI(i)	
10	R2	GPIO1[10](io)	SPI1_S_MISO(o) / SPI1_M_MISO(i)	
11	P2	GPIO1[11](io)	SPI1_M_C(o) / SPI1_S_C(i)	
12	N3	GPIO1[12](io)	GPIO1[12](io)	
13	M4, J14(LED_B)	GPIO1[13](io)	GPIO1[13](io)	
14	D5, R3(LED_R)	GPIO1[14](io)	GPIO1[14](io)	
15	D6, P13(LED_G)	GPIO1[15](io)	GPIO1[15](io)	

13. PWM (Pulse Width Modulation controller)

13.1. Specification

8bit pre-scaler.

16bit high / low level counters.

16bit pulse counters.

Channel : 4ch

13. PWM (Pulse Width Modulation controller)

13.2. Register map

Address	Register	Function	Initial value	Note
10016000h 10016100h	PRE_SCALER[7:0]	[7:0]:Pre-scaler - 1 Frequency=Clock frequency/(PRE_SCALER+1)	00h	Clock frequency is 32MHz.
10016004h 10016104h	ENABLE[3:0]	[3:0]:Enable 0-Disable 1-Enable	0h	
10016008h 10016108h	REVERSE[3:0]	[3:0]:Reverse 0-Normal 1-Reverse	0h	
1001600Ch 1001610Ch	RUN[3:0]	[3:0]:Run/Stop 0-Stop 1-Run	0h	
10016010h 10016110h	HIGH0[15:0]	[15:0]:High level count - 1	0000h	
10016014h 10016114h	LOW0[15:0]	[15:0]:Low level count - 1	0000h	
10016018h 10016118h	COUNT0[15:0]	[15:0]:Pulse count	0000h	
1001601Ch 1001611Ch	HIGH1[15:0]	[15:0]:High level count - 1	0000h	
10016020h 10016120h	LOW1[15:0]	[15:0]:Low level count - 1	0000h	
10016024h 10016124h	COU1[15:0]	[15:0]:Pulse count	0000h	
10016028h 10016128h	HIGH2[15:0]	[15:0]:High level count - 1	0000h	
1001602Ch 1001612Ch	LOW2[15:0]	[15:0]:Low level count - 1	0000h	
10016030h 10016130h	COUNT2[15:0]	[15:0]:Pulse count	0000h	

13. PWM (Pulse Width Modulation controller)

Address	Register	Function	Initial value	Note
10016034h 10016134h	HIGH3[15:0]	[15:0]:High level count - 1	0000h	
10016038h 10016138h	LOW3[15:0]	[15:0]:Low level count - 1	0000h	
1001603Ch 1001613Ch	COUNT3[15:0]	[15:0]:Pulse count	0000h	

14. ADC (Analog Digital Converter)

14.1. Specification

125KS/s (Select 8ports analog ports and convert continuous)

Channel : 8ch

14.2. Register map

Address	Register	Function	Initial value	Note
10017000h	ADC0[11:0](R)	[11:0]:ADC value	xxxx	
10017004h	ADC1[11:0](R)	[11:0]:ADC value	xxxx	
10017008h	ADC2[11:0](R)	[11:0]:ADC value	xxxx	
1001700Ch	ADC3[11:0](R)	[11:0]:ADC value	xxxx	
10017010h	ADC4[11:0](R)	[11:0]:ADC value	xxxx	
10017014h	ADC5[11:0](R)	[11:0]:ADC value	xxxx	
10017018h	ADC6[11:0](R)	[11:0]:ADC value	xxxx	
1001701Ch	ADC7[11:0](R)	[11:0]:ADC value	xxxx	